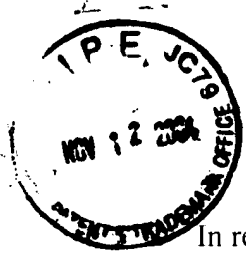


IFW



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:
Taddiken

MMB Docket No. 1890-0079

Application No. 10/826,921

Filed: April 16, 2004

For: Semiconductor Structure Having
a Compensated Resistance in the
LDD Area and Method for
Producing the Same

Examiner: To be assigned

Group Art Unit: 2811

I hereby certify that this correspondence is being deposited
with the United States Postal Service as first class mail in
an envelope addressed to: Commissioner for Patents, P.O.
Box 1450, Alexandria, VA 22313-1450 on

November 9, 2004

(Date of deposit)

James D. Wood

Name of person mailing Document or fee

Signature

November 9, 2004

Date of Signature

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, Applicant hereby discloses the following references
regarding the above-identified patent application.

Articles

- 1) Gebara, Edward, Niklas Rorsman, Jörgen Olsson, Herbert Zirath, Klas Håkan Eklund, "Output Power Characteristics of High Voltage LDMOS Transistors," Proceedings of the 5th Symposium on Gigahertz Electronics, Goeteborg, Sweden, March 2000, pages 75-78, (4 pages).

- 2) Disney, D. R., A. K. Paul, M. Darwish, R. Basecki, V. Rumennik, "A New 800V Lateral MOSFET With Dual Conduction Paths," Proceedings of the 13th International Symposium on Power Semiconductor Devices & ICs, Osaka, Japan, June 2001, pages 399-402, (4 pages).
- 3) Cai, Jun, Changhong Ren, N. Balasubramanian, Johnny K. O. Sin, "A Novel High Performance Stacked LDD RF LDMOSFET," IEEE Electron Device Letters, Vol. 22, No. 5, May 2001, (3 pages).
- 4) Söderbärg, A., B. Edholm, J. Olsson, F. Masszi and K. H. Eklund, "Integration of a Novel High-Voltage Giga-Hertz DMOS Transistor into a Standard CMOS Process," IEEE, 1995, pages 38.5.1-38.5.4, (4 pages).

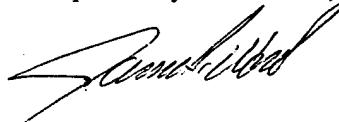
"Output Power Characteristics of High Voltage LDMOS Transistors," "A New 800V Lateral MOSFET With Dual Conduction Paths," and "A Novel High Performance Stacked LDD RF LDMOSFET," were cited in a International Preliminary Examination Report (English translation enclosed) in a related Foreign patent application number PCT/EP02/09702 filed on August 30, 2002.

Pursuant to 37 C.F.R. § 1.97(b), this Information Disclosure Statement is being filed within three months after the filing date of the application or before the mailing of the first office action on the merits.


It is believed that no fees are due for the consideration of this Information Disclosure Statement. However, the Commissioner is hereby authorized to charge any deficiency or to credit any overpayment to Deposit Account No. 13-0014, but not to include any payment of issue fees.

November 9, 2004
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111 Monument Circle, Suite 3000
Indianapolis, Indiana 46204-5115
(317) 638-2922

Respectfully Submitted,



James D. Wood
Attorney for Applicant
Registration No. 43,285

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT 	MMB DOCKET NO. 1890-0079	APPLICATION NO.: 10/826,921
	APPLICANT(S): Taddiken	
	FILING DATE: April 16, 2004	GROUP ART UNIT: 2811

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
-	AA						
	AB						
-	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL						Yes No
	AM						Yes No
	AN						Yes No
	AO						Yes No
	AP						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AQ	1	Gebara, Edward, Niklas Rorsman, Jörgen Olsson, Herbert Zirath, Klas Håkan Eklund, "Output Power Characteristics of High Voltage LDMOS Transistors," Proceedings of the 5 th Symposium on Gigahertz Electronics, Goeteborg, Sweden, March 2000, pages 75-78, (4 pages).
	AR	1	Disney, D. R., A. K. Paul, M. Darwish, R. Basecki, V. Rumennik, "A New 800V Lateral MOSFET With Dual Conduction Paths," Proceedings of the 13 th International Symposium on Power Semiconductor Devices & ICs, Osaka, Japan, June 2001, pages 399-402, (4 pages).
	AS	1	Cai, Jun, Changhong Ren, N. Balasubramanian, Johnny K. O. Sin, "A Novel High Performance Stacked LDD RF LDMOSFET," IEEE Electron Device Letters, Vol. 22, No. 5, May 2001, (3 pages).

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicants.

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	MMB DOCKET NO. 1890-0079	APPLICATION NO.: 10/826,921
	APPLICANT(S): Taddiken	
	FILING DATE: April 16, 2004	GROUP ART UNIT: 2811

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	BA						
	BB						
	BC						
	BD						
	BE						
	BF						
	BG						
	BH						
	BI						
	BJ						
	BK						
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	BL						Yes No
	BM						Yes No
	BN						Yes No
	BO						Yes No
	BP						Yes No
OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	BQ	<u>2</u>	Söderbärg, A., B. Edholm, J. Olsson, F. Masszi and K. H. Eklund, "Integration of a Novel High-Voltage Giga-Hertz DMOS Transistor into a Standard CMOS Process," IEEE, 1995, pages 38.5.1-38.5.4, (4 pages).				
	BR	<u>2</u>					
	BS	<u>2</u>					
EXAMINER					DATE CONSIDERED		
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicants.							